Self-Assembled Metallic Nanowire-Based Vertical Organic Field-Effect Transistor

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Ⓢ Supporting Information

ABSTRACT: We report on in situ, self-assembly, solution-processing of metallic (Au/Ag) nanowire-based transparent electrodes integrated to vertical organic field-effect transistors (VOFETs). In the VOFET architecture, the nanowires' microstructure facilitates current modulation by the gate across the otherwise shielding sandwiched source electrode. We show N-type VOFETs operation with on/off ratio $\sim 1 \times 10^5$ and high current density (>1 mA cm^{-2} at V_{DS} = 5 V). The integration of the device design and the transparent electrode deposition methods offers a potential route for all-solution processing-based, large-area, high-efficiency organic electronics.

KEYWORDS: nanowires, self-assembly, vertical FETs, organic electronics, transparent electrodes
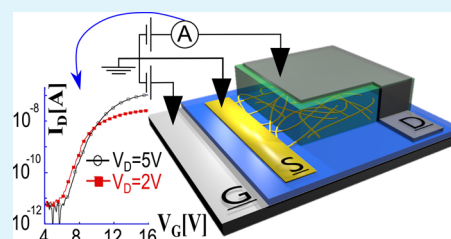
Solution-processed materials for optoelectronics and organic electronics attract great interest because of their compatibility with low-cost and large-area manufacture processes.[1] These merits encourage research of solution-processed functional materials that enable new lighting, display, energy harvesting, sensing, and logic applications.[2−6] Although there is a wide selection of such substrates, insulators, semiconductors, and conductors, solution-processable, flexible, transparent eElectrodes (TEs) still struggle to reach the industrial figures of merit of transparent conductive oxides.[7] Numerous optoelectronic devices require TEs; such devices commonly feature a vertical architecture in which the photoactive material is sandwiched between two conductive layers, as with the case of standard light-emitting diodes (LEDs) and solar cells. But the functionality of nonoptical electronic devices that are characterized by vertical architecture is also based on TEs. Two main groups of such devices are the solid state triodes[8] (also referred to as space-charge-limited transistors[8,9]) and the more recently developed vertical field-effect transistors (VFETs).[10−16]

A key feature in the VFET is that its sandwiched source electrode would be transparent to DC electric fields so that the gate could affect the channel region. Transparency to visible light could be a bonus in some applications but it is not a must. When one is interested in extending the transparency to frequencies well below the optical spectrum or even to DC electric fields, only structured films seem to be a promising platform. These include graphene and metallic grated films, or solution-deposited carbon nanotubes (CNT) and metallic Nano-Wires (NWs) films.[12,13,17] CNT films tend to suffer from relatively high sheet resistance and due to their deposition technique also tend to form high surface roughness. Metallic NWs proved to be attractive because of their low sheet resistance,[18] and it has been shown that they can be implemented using a variety of metals (e.g., Cu, Ag, Au, etc.), size scales, and deposition processes.[19−21] However, such metallic NWs films would typically also suffer from surface roughness that may make them impractical as electrodes for ~100 nm scale thick devices. We show that using a controlled synthesis of Au NWs may turn this technology one of the enabling technologies for VFETs.

To establish a better understanding of design constraints and to explain the need for nanostructured low-roughness transparent electrode, we first describe the VFET architecture and the physics that governs its operation. The 3D illustration of the vertical FET architecture is shown in Figure 1a, and its cross-section is shown in Figure 1b. The VFET consists of the following stack of layers: gate (G), gate dielectric, source electrode (S), a semiconductor, and a top drain contact (D). This architecture has the advantage for facile fabrication of ultrashort channel length devices, as the channel length is simply determined here by the semiconductor layer's thickness. However, the source electrode, which is sandwiched between the gate and the semiconductor, introduces significant shielding effects, similar to a Faraday cage. A source electrode made of high quality conductors such as metals, where the Debye
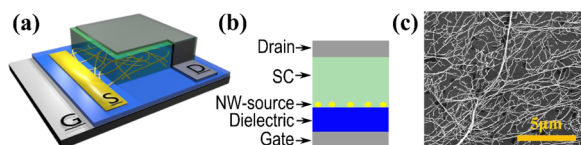
Figure 1. (a, b) Illustration of the Au/Ag Metallic NW-based VOFET (MN-VOFET) architecture. The metallic NW film serves as the embedded transparent electrodes between the bottom gate, gate dielectric layers, and the upper semiconductor and drain layers. (c) High-resolution scanning electron microscopy (HRSEM) of a metallic NWs film (indicated with bright color).

shielding length can be approximated to the atomic scale, may completely separate the VFET into two functional parts: a capacitor below the source, and a diode above it. To allow these parts to interact, the source electrode has to be transparent to the low-frequency or DC vertical gate electric fields. As discussed in previous works[14,22−24] and demonstrated both theoretically and experimentally, that nanostructured or gridlike shaped films can achieve this type of transparency. Namely, the type of VFET discussed here is the patterned electrode (source) VFET.[13]

As expected, the physical underpinnings of the VFET's operation differ from those of its lateral counterpart. The VFET is governed by several mechanisms, which we addressed in depth in references[24] and.[25] The very basic mechanism, which we term as the virtual contact formation, relies on a high potential-barrier between the source and the semiconductor to minimize direct source-drain currents at Off state (Schottky barrier contact). In the on state, gate electric fields diminish the Schottky barrier; they penetrate into the openings in the source electrode and induce charge injection and formation of regions saturated with mobile charge carriers, which can now flow toward the drain. With that, the source electrode film (and in microscale view the perforation regions) behaves as an ohmic contact, and is no longer considered a current limiting factor.[23] This charge accumulation at the openings in the source electrode (i.e., the virtual contact) is confined by the metallic source electrode perforations' "walls", hence the high significance of these regions' aspect ratio (source thickness to perforation size). In fact, this parameter is so important that any

slight change in the aspect ratio directly translates to a significant variation in the device's performance. For example, we previously demonstrated that a 5% variation in the aspect ratio resulted in an order of magnitude change in the device on/off ratio.[24]

However, the effect of rough electrodes extends beyond the direct influence of the aspect ratio on the device performance. In practice it could also reduce the effective film thickness promoting high Off currents, and at the extreme, may also lead to pinholes formation between the source and the drain. Given we aim at sub 100 nm channel length (active layer thickness) devices, a fine-tuned nanostructured electrode fabrication is a necessity. We found that controlling the NWs self-assembly initiation process is the key point to achieve layer uniformity that would allow for reproducible results. Thus, instead of using protocols using borohydride as the catalytic initiator,[19] we followed a work reporting the synthesis of metal NWs from preprepared catalytic nanogold seeds.[26] This by itself was not enough and we achieved further reduction in the film roughness by lowering the NWs' surface density, using lower (×3) concentration solutions. The resulting film was characterized using AFM as shown in Figure 2. The maximum NWs film height is found to be below 30 nm (Figure 2a, b), a typical width of a NW bundle is about 100 nm (Figure 2c, d), and the distance between bundles is a few hundreds of nanometers. Comparing with the design rules in ref 23 and 25, the distance between the bundles corresponds to the diameter (D) of the hole in the electrode and the height corresponds to the electrode thickness (h). The aspect ratio of h/D achieved here is low enough to allow for a high on/off ratio.[23,25]

Following the formation of the NWs electrode on the Si/SiO$_2$ substrate (100 nm SiO$_2$ as gate insulator) we completed the VFET structure by depositing an active layer and Al top contact. The overlap between the three electrodes defines the device area that here is about 1×10^{-4} cm^2 (more details are in the Supporting Information). On the basis of the improved NWs film properties we were able to use a thin active layer as the polymer P(NDI2OD-T2) (Polyera, ActivInk N2200) that was spin coated (12 mg/mL chloroform at 4k rpm) to ∼100 nm thick layer. The choice of this polymer was made due to several reasons. It can be deposited from orthogonal solutions
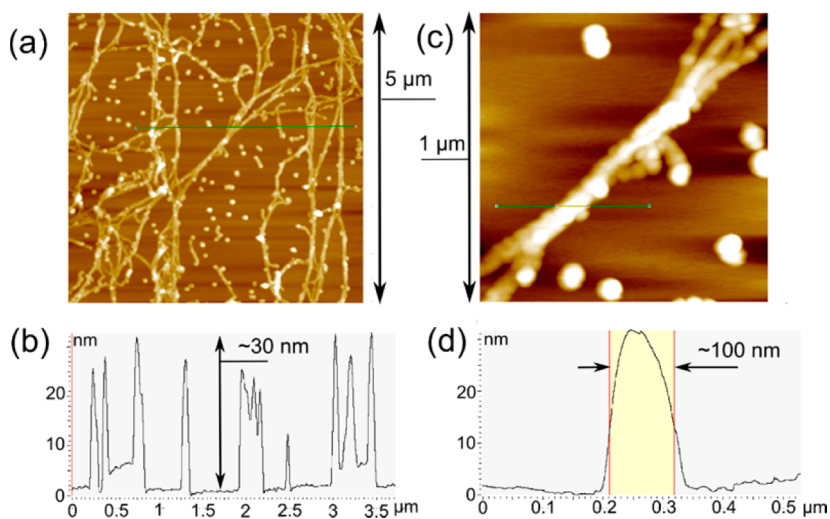
Figure 2. AFM image of the nanowires film after the second stabilization dipping step: (a) 5 × 5 μm image. (b) Cross-section along the line sown in a. (c)Zoom on a single NW bundle. (d) Cross-section along the line shown in c.
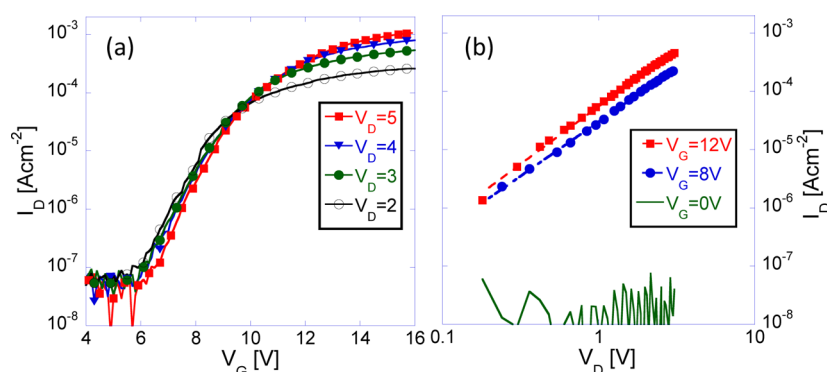
Figure 3. I−V characteristics of vertical FETs based on the N2200 polymer. (a) Transfer characteristics, I_D−V_G .(b) Output characteristics, I_D−V_D. The dashed lines in b are power-law fits.

(chloroform) to the NWs film. It is an n-type air-stable semiconductor and its LUMO level (∼4 eV) should be sufficiently distanced from the NWs' work function. Examining the device transfer characteristics shown in Figure 3a, one can immediately spot several key features. The VFET turns on at about V_G = 5.5 V and below that the current is negligible and very close to our measurement setup resolution (pA). At the vicinity of the turn-on voltage the drain bias has very little effect on the current. The suppression of the direct effect of the drain voltage also results in an on/off ratio approaching 1×10^5. Turn on slope is reasonable for this structure (SS = 1 V/dec) and the current saturates at approximately V_G = 12 V. Figure 3b shows the output ($I_D − V_D$) characteristics of the VFET where for the gate bias of 8 and 12 we fitted the data to a power law function (dashed lines). The power law for gate bias of 8 and 12 was found to be 1.9 and 2, respectively. This indicates that the gate has indeed turned the source contact into an ohmic one making the current voltage characteristics space charge limited.[23,25]

To summarize, this work highlights the potential of using a random network of metallic NWs as the source electrode for low-cost vertical FETs. We demonstrated a process showing how judicial choice of the NWs synthesis protocol as well as the active semiconducting materials can result in high performance n-type devices featuring high on/off ratio ($>1 \times 10^4$), high driving current density (1×10^{-3} A cm^{-2} at V_{DS} = 5 V), and reasonable subthreshold slope (∼1 V/dec). In future work, we aim to integrate NWs with intermediate diameter (∼8 nm) in our devices: With much higher fill factor because of their nonbundled assembly, they retain a similar visible spectrum transparency but, at the same time, we expect them to provide a superior low-frequency electric field transparency. Thus, we strongly believe that having demonstrated solution-processed, smooth, and transparent NW electrodes constitutes a key milestone in enabling lithography-free, ultrashort channel length devices for low-cost and highly efficient organic electronics.

ASSOCIATED CONTENT

Ⓢ Supporting Information

Experimental section (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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